TWIN-CELL FLASH MEMORY STRUCTURE AND METHOD

Abstract of the Disclosure

A programmable memory cell structure that includes a pair of memory cells is provided. Each pair of memory cells includes a shared control gate and first and second floating gates present about the shared control gate. The first and second floating gates have respective gate regions disposed on respective sides of the control gate. Dielectric structures are present between the control gate and respective ones of the gate regions of the floating gates. The control gate and gates of the first and second floating gates are formed within a single lithographic square.